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A Survey on 100MHz High Resolution Digitization System

Ganesh Vijay More

PG Student [VESIT], Dept. of Instrumentation Engineering, VESIT, Chembur, Mumbai, India

ABSTRACT: Nowadays high speed Data Converters is increasingly needed. An application involving high-speed data acquisition systems puts pressure on the analog to digital interface data rate also. The high sampling rate of the Analog to Digital Converters (ADC) demands the use of advanced acquisition techniques as well as the latest technology available. This paper presents a survey on a high speed Digitization technique along with components selection.. The aim is to develop high speed digitization system. It also discusses the types of high speed ADCs along with their advantages and disadvantages. The important parameter of the digitization system is speed of conversion or sampling rate. So for development of high speed Digitizer system, one should choose a proper high speed Analog to Digital Converter based on the application requirements. The main blocks of the system are high speed ADC, FIFO memory, Clock Generator & Multiplier. For storing high speed data; FIFO is used as a temporary storage element. The designed system efficiency can be increased by storing only valid data and reject unwanted data.

KEYWORDS: High Resolution, Digitization System, High Speed ADC etc.

I.INTRODUCTION

Digitizer is an embedded system which has wide application in real time monitoring, communication, data transmission, image data acquisition, radar, telemetry, remote sensing etc. The main process involved in digitization system is to convert analog signal to digital signal that can be processed by various systems and then sent to the computer for real time monitoring. Its accuracy, reliability and versatility make it prominent to play a leading role in modern electronic instruments.
It involves collection of data for the purpose of analysis or documentation of some process. Data conversion using electronic equipment's increases the accuracy and reliability. Analog to digital converter is the main part of the system as it determines the resolution which in turn fixes the speed of the Digitization system. The data that may be in analog or digital form are read, filtered, processed and sent to different displaying devices using proper interfaces. In microcontroller based systems the processing is done using the microcontroller unit. The main advantages of this system are its low cost, low power consumption and smaller size.
The last couple of decades had witnessed a steep rise in extensive research for High Speed Digitization Systems. This resulted in applications focused initially in military, aerospace equipments and later in Medical Imaging Technology and various engineering fields.

II.LITERATURE SURVEY

Manoj Kumar Dey, and Sandeep Dattaprasad (2012) presented Architecture and Design of High Speed Data Acquisition System. They have presented analysis and proposed a simple principle and structure for designing Data Acquisition hardware system with use of Field Programmable Gate Arrays (FPGAs). In that a hardware system employing architecture uses E2V's Analog to Digital Converters (ADC), Alteras Stratix III and Cyclone II FPGAs and Samsung's 1Gb DDR3 memory devices for data storage[1].

Robert Finger(Texas Instruments (2001)) had presented Application report on design for interfacing TI high speed Data converters to DSP's using FIFO's.The application report shows how to use two SN74V2x5 FIFOs as an interface

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between TMS320C6201 and TMS320C6203 DSPs and a THS1031 analog-to-digital converter or THS5661A digital-to-analog converter. This method can also be used for other data converters[2].

Anju P. Raju and Ambika Sekhar(2012) presented a Implementation of High Speed Distributed Data Acquisition System. This system is based on Field Programmable Arrays(FPGA). They have developed High Speed Distributed Data Acquisition System which is a multichannel analog data acquisition system, acquires data from 16 analog channels and transmits the captured data to the displaying device through Ethernet device. Control logic unit implemented in the FPGA controls and coordinates the action of the various devices involved in data acquisition [3].

Nie Hongshan and Wang Yinan(2011) presented the hardware model of High Speed Real-Time Data Acquisition System Based on Solid-state Storage Technique. This hardware system mainly consists of data acquisition, distribution and storage section. They had used 3GSPS ultra high-speed ADC which is applied in acquisition section. In distribution section, the original data stream is distributed into four streams. Each data stream is stored into one solid-state storage card which is composed of NAND flash array. Also, In aspect of software, implementation methods of DDR3-based FIFO and NAND flash controller were introduced in detail[4].

III.TYPES OF HIGH SPEED ADC

1. **Flash ADC**
2. **Pipelined ADC**

(1)Flash ADC

Flash ADCs (sometimes called parallel ADCs) are the fastest type of ADC and use large numbers of comparators. An N-bit flash ADC consists of 2^Nresistors and 2^N-1 comparators arranged as in Figure 2.6. Each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a 1 logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a 0 logic output. The 2^N-1 comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a thermometer code. Since 2^N-1 data outputs are not really practical, they are processed by a decoder to generate an N-bit binary output. However, the architecture uses large numbers of resistors and comparators and is limited to low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators (especially at sampling rates greater than 50 MSPS), and relatively large (and therefore expensive) chip sizes[5].

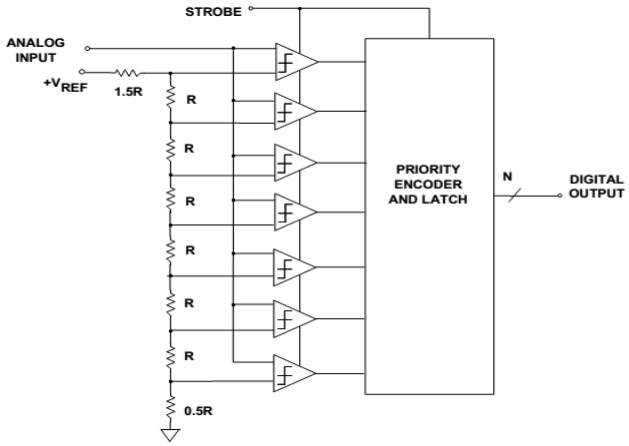

Fig.(a): Flash ADC[5]

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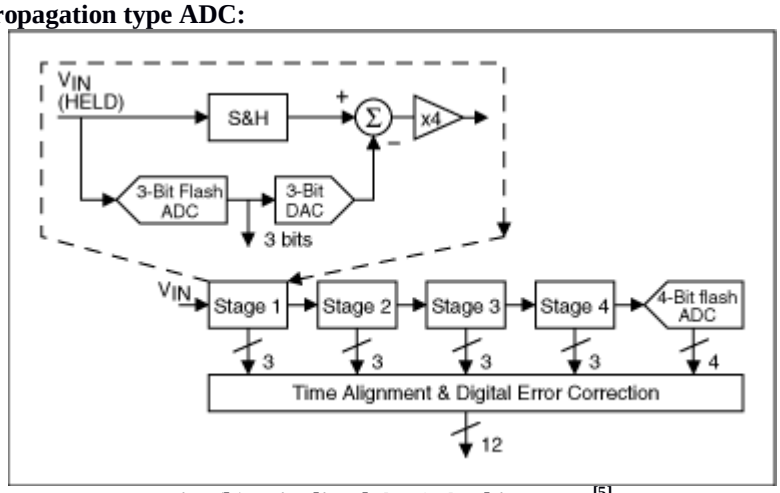
Advantages:

- Flash converters are capable of high sampling rates up to 1GSPS.

Disadvantages:

- Design limitations on higher resolution (limited to 8-bits).
- More power consumption due to large number of resistors and comparators**.**

(2)Pipelined or Propagation type ADC:



- **Fig. (b): Pipelined ADC Architecture [5].**

In this schematic, the analog input, V_{IN}, is first sampled and held steady by a sample-and-hold (S&H), while the flash ADC in stage one quantizes it to three bits. The 3-bit output is then fed to a 3-bit DAC (accurate to about 12 bits), and the analog output is subtracted from the input. This ”residue” is then gained up by a factor of four and fed to the next stage (Stage 2). This gained-up residue continues through the pipeline, providing three bits per stage until it reaches the 4-bit flash ADC, which resolves the last 4LSB bits. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic. Note when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput. Less popular type of error corrected subranging architecture is the recirculating subranging ADC. The concept is similar to the error corrected subranging architecture previously discussed, but in this architecture, the residue signal is recirculated through a single ADC and DAC stage using switches and a programmable gain amplifier (PGA). The major problem with this technique is the PGA. Its gain bandwidth product will limit the frequency response at higher gains. Also matching of the various gains could be problematic [5].

Advantages:

• Higher Sampling rates can be achieved, i.e. up to 550MSPS.

• As high sampling rate can be achieved, higher Bandwidth signals can be digitized.

Disadvantages:

• Pipeline ADC requires external clock signal to start conversion.

• Processing of signal is done at every stage of pipelined architecture, it generates Pipeline delay.

IV.SYSTEM DESCRIPTION

Now days in analog signal-processing system, there is often the need for high-speed digitization. Connecting fast data converters to a DSP can be a demanding task. The high speed A/D converters designed for digitizing high frequency, wide dynamic range signals. They are perfect for demanding communications applications with AC performance. As

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data conversion will be at high speed, so high speed FIFO is an ideal solution to buffer some of output data. When a whole block of data has been sampled, the data can be transferred in a read burst from the FIFO to the PC using USB based PC Interface for further processing [2].

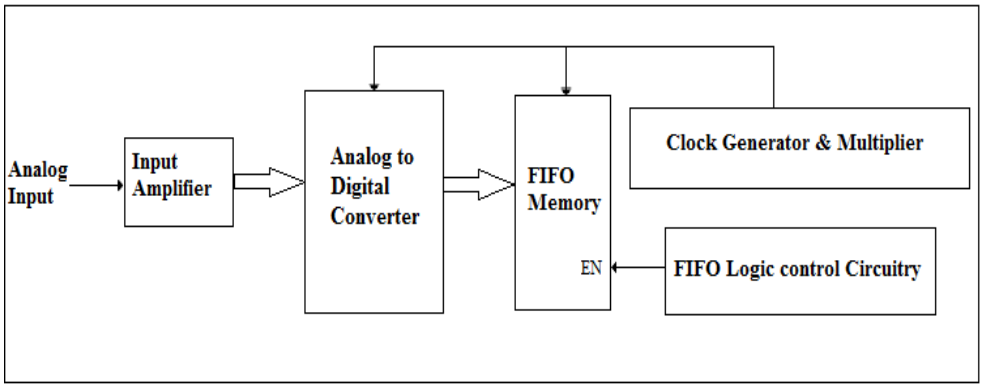

Fig.(c): Block Diagram of System.

Here as shown in above block diagram, at start analog input is amplified according to ADC input specifications and then given to high speed ADC. The high speed clock is generated by the clock generator & multiplier and given to ADC and FIFO. The input signal is sampled and converted into digitized form by ADC at high rate.
At the speed of several MHz instantaneous data transfer to PC is difficult so First-In-First-Out(FIFO) memory is used as temporary storage element for high speed operations. Digital data is first stored in FIFO; and this data is then transfer to PC for processing or displaying.
All the input signal may not be of interest, so unwanted signal should be rejected or should not be stored in the FIFO. The FIFO Logic Control Circuitry is used for FIFO to store only signal of interest not the unwanted signal. This OFF time of FIFO can be used for data transfer; due to this one can simultaneously read and write data. Therefore, FIFO will never be overflow.

V. SYSTEM DESIGN

Selection of components is most important task, as every component should be capable of high speed operation. Major components required for the system are:
•Analog to Digital Converter
•Input Amplifier
• Clock Generator & Multiplier
• FIFO Memory

Analog to Digital Converter:
In high speed digitization system ADC is the most important component. The main parameters of ADC need to be considered for selections are Sampling Rate, Conversion Time and Resolution. For high speed digitization, Sampling Rate of ADC should be high. As sampling rate increases more data will be converted in finite time. Thus required sampling rate should be in several Mega Samples per Seconds (MSPS).
Conversion time is the time required for ADC to digitize one input sample. Therefore ADC's having very low conversion time are preferred for high speed operations. Another factor to be considered is Resolution. Resolution of the converter indicates the number of discrete values it can produce over the range of analog values. For precise and accurate measurement resolution of the converter should be high.
The output type (Serial or parallel) of ADC also affects speed of operation. In serial mode, ADC requires one clock Cycle to output one bit. For all bits to appear at output, it takes that number of clock cycles. In parallel output, for all the bits to available at output ADC requires only one clock cycle. So according to application requirements proper ADC should be selected.

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As from the above requirements Linear Technology's LTC2145 high speed Propagation type ADC with 12-bit Resolution and sampling rate of upto 125MSPS is used for this application.

Input Amplifier:
Input to the amplifier is a continuous changing low level signal. As it is a random, input signal amplitude may take any values. For selecting input amplifier ADC specifications should also be taken into considerations. ADC has fixed range of input signal, beyond its absolute maximum ratings of input signal ADC may damage. This will create a problem; So to limit the input signal level up to ADC's maximum ratings there should be a provision. This can be done by using amplifier at the input of ADC which limits the input signal corresponding to ADC maximum rating value. For restricting input signal, supply voltage of amplifier should be same as supply voltage of ADC, as utput of op-amp will never exceeds its supply voltage. This will automatically limit the input signal level of ADC. Bandwidth of op-amp is also the key parameter for selection of amplifiers. For high speed operations bandwidth of op-amp should be high.

Texas Instruments LMH6629 Ultra-Low Noise, High-Speed Operational Amplifier, having input bandwidth of 900MHz is used in this application.

Clock Generator & Multiplier:
A clock generator is a circuit that produces a timing signal (also known as a clock signal), for use in synchronizing a circuit's operation. This clock signals are used for synchronizing operation of ADC and other circuitry. Sampling rate of ADC is decided by clock signal frequency. In general Sampling frequency is equal to clock signal frequency supplied to ADC. To achieve high sampling rate(up to several MSPS), clock generator should be capable of providing that much high frequency clock signal. Instead of generating high frequency clock signal, we can generate a fixed frequency clock signal using clock oscillators and then its frequency can be multiplied by different factors to achieve clock signals of various frequency . This can be done by programmable clock multipliers. This gives us advantage of achieving different sampling rate using same circuit. The important factor that should be considered during selection of clock generator & multiplier is Jitter. Jitter is the deviation from true periodicity of a presumed periodic signal. The time between every two samples should be same, if the jitter is present on the clock signal to ADC then time between samples varies and instantaneous error arises. So clock source selected should be jitter free.

The crystal oscillator MXO45HST-20M having fixed output frequency of 20MHz which is then multiply by clock multiplier IDT501. Clock multiplier can produce frequencies up to 160MHz. These both selected oscillator and multiplier are used for this application to get high frequency clock signal.

FIFO Memory:
First In First Out(FIFO) is a type of memory generally used as temporary storage element. It works on First In First Out principle. Selection of FIFO is mainly based on its Access Time, Read-Write cycle Time and Memory Locations. Access time is the time required for FIFO to perform one single operation.As output of ADC is coming at high rate(at several MHz), so FIFO should be able to store every sample. To store every sample coming at high rate, access time of FIFO should be small enough to . After storing every data at high speed, it can be then transfer to PC. Input and output type of FIFO(i.e. Serial or Parallel) is also one of the criteria to select FIFO for high speed operations. For serial input and output, it takes one clock cycle to read or write one bit of data that means, to read or write n-bits FIFO will take 'n' no. of clock cycle. This will reduce speed of operation. While on the other hand, in case of parallel input and output, only one clock cycle will be require to read or write all n- bits of data which increases reading and writing speed. So FIFO should have Parallel-In & Parallel-Out for high speed operations.

For storing data Texas Instruments SN74V245 FIFO, having 4096X18 bits of memory with access time of 5nsec is used in this system.

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VII.CONCLUSION

The design and development of high speed digitization system is completed. It can be used for evaluation of different types of analog inputs having high rise time. This system is highly reliable and portable and hence can be used for data acquisitions at places such as laboratories, workshops, and other remote places. Compared to conventional data acquisition cards the designed system is low-cost, high speed, and real-time.

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